"FLOATING POINT ALU 32 BIT USING VHDL SIMULATION"

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ABSTRACT: *A floating point arithmetic and logic unit design using pipelining is proposed. By using pipeline with ALU design, ALU provides a high performance. With pipelining plus parallel processing concept ALU execute multiple instructions simultaneously. Floating point ALU unit is formed by combination of arithmetic modules (addition, subtraction, multiplication, division), Universal gate module. Each module is divided into sub-module. Bits selection determines which operation takes place at a particular time. The design is and validated using vhdl simulation in the xilinx13.1i software.*

Keyword*:* Arithmetic logic unit, floating point

1. INTRODUCTION

Floating point describes a system for representing numbers that would be too large or too small be represented as integers. Floating point representation is able to retain its resolution and accuracy compared to fixed point representation. IEEE specified standard for floating-point representation known as IEEE 754 in 1985.

The IEEE 754 floating point format consists of three fields.

Sign bit: 1 bit .It is 1 for a negative number and 0 for positive number.

Exponent: 8 bits. The exponent represents a power of two.

Mantissa: Final portion of word (23 bits) is the significant that is also called as mantissa. Mantissa is a Fractional part. Arithmetic logical unit is a combinational network that performs arithmetic and logical operation on the data. For computation input data is given to A.L.U. code is also given from control unit, according to that code it compute the result. The ALU with floating point operations is called a FPU.
Pipelining plus parallel processing execute is used to execute multiple instructions simultaneously. The cycle time of the processor is reduce .If pipelining is use, the CPU Arithmetic logic Unit can be design faster. It increases the overall performance of a system. In the floating point ALU with universal logic gate we can perform addition, subtraction, multiplication, division operation and logical operation with less delay and less area.

2. MOTIVATION

Floating-point calculation is very important subject. This is surprising, because floating-point is omnipresent in computer systems. Floating-point (FP) data type is almost present in every language. From PCs to supercomputers, all have FP accelerators in them. Most compilers are called from time to time to compile the floating-point algorithms and virtually every OS have to respond to all FP exceptions during operations such as overflow. Also FP operations have a direct effect on designs as well as designers of computer systems. So it is very important to design an efficient FPU such that the computer system becomes efficient. Here we are designing 32 bit floating point A.L.U. which perform arithmetic operation which include addition ,subtraction, multiplication , division, logical operation and design of universal logic gate with high accuracy, high speed ,less delay and less area.

3. LITERATURE REVIEW

By referring first this paper 16 bit floating point ALU is design using pipelining. Pipelining is use to execute multiple instructions simultaneously .Top-Down design approach is use. In top-down design approach, four arithmetic modules, addition, subtraction, multiplication and division are combined to form a floating point ALU unit. Each module is divided into sub- modules. Two selection bits are combined to select a particular operation. Each module is independent to each other .all modules in the ALU design are realized using VHDL, design functionalities are validated through VHDL simulation .all components and module is successfully run, Synthesis and Simulation in the Xilinx. The problem in this ALU is that

hardware complexity in terms of synthesis is more. **[1]** 32 bit floating point ALU is design using pipelining. The design approach is same as that of design of 16 bit ALU. Concept of pipelining is use to execute multiple instruction simultaneously. Top down approach is also use. It performs four operations, Addition, subtraction, Multiplication and Division. Each module is independent to each other, all modules in the ALU design are realized using VHDL, design functionalities are validated through VHDL simulation .All components and module is successfully run, Synthesis and Simulation in the Xilinx. The problem in this ALU is that hardware complexity in terms of synthesis is more. **[2]**

A floating point arithmetic and logic unit design using pipelining. By using pipeline with ALU design, ALU provides a high performance. With pipelining concept ALU execute multiple instructions simultaneously. Top-Down design approach is use. Floating point ALU unit is formed by combination of arithmetic modules (addition, subtraction, multiplication, division), logical operation module (AND, OR, NOT). Each module is divided into sub-module is shown in fig.1.Bits selection determines which operation takes place at a particular time. The design is and validated using vhdl simulation in the xilinx12.1i software. The problem in this ALU is that hardware complexity in terms of synthesis is more**.[3]**

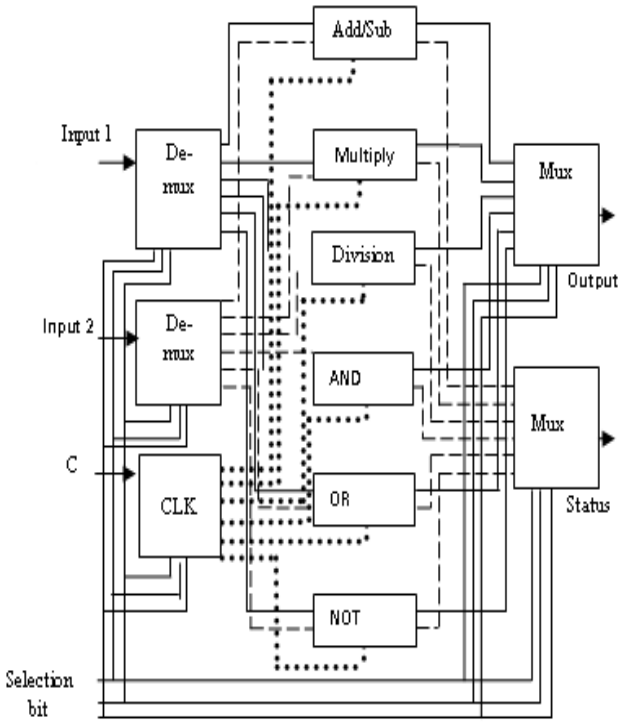

Figure 1: Top view of A.L.U. design

32 bit floating point ALU is design. Floating point operations are hard to implement on Field Programmable Gate Arrays (FPGA) because of the complexity of algorithms is more. Then again, many scientific applications require floating point arithmetic because of high accuracy in their calculations. In this paper an efficient implementation of an IEEE 754 single precision floating point arithmetic unit is designed in Xilinx SPARTAN 3E FPGA. VHDL environment is performed for floating point arithmetic unit design using pipelining, which provides high performance. Pipelining is used to execute multiple instructions simultaneously. In top-down design approach, four arithmetic modules, addition/ subtraction, multiplication and division are combined to form a floating point arithmetic unit. FP addition is implemented using Leading-One-Detector (LOD), Leading-One-Predictor (LOP) and two-path algorithms. In this ALU for Adder module clock period is (LOD- 33.159ns, LOP-28.358ns, Tow-path- 22.313ns), for FP multiplier it is 10.402 ns, for FP divider it is 7.058ns. And the area in slices is for Adder module it is (LOD- 694, LOP-731, Two- path- 1020), for FP multiplier it is 272, for FP divider it is 185. Synthesis and simulation results are obtained by using Xilinx13.1i platform. **[4]**

4. OVERALL ANALYSIS OF REPORTED WORK

From the overall analysis we can say that floating point ALU was design that performed arithmetic operation which include addition, subtraction, Multiplications, and Division operations. That ALU was designed using pipelining because of that that the speed of ALU is increases and it executes multiple instructions simultaneously. That ALU was designed with Top down approach .In that ALU problem is that a more delay, more area, and hardware complexity in terms of synthesis is also more. This conclusion is made in [1], [2] and [4].After that one ALU was designed that performed Addition, subtraction, multiplication, division, AND, OR, NOT operation [3]. Same designing method was used .Same problem is present in this ALU also. Our approach is that to design 32 bit floating point ALU with universal logic gate, which can perform Addition, subtraction, multiplication ,division , Logical operation with less delay and less area.

5. PROBLEM DEFINITION

An A.L.U. performed addition, subtraction, multiplication, and division operation, latter on this, they add the logical operation which include AND, OR, NOT gate but the hardware complexity in terms of synthesis, delay and area is also more with less accuracy. So to avoid this problem we are designing 32 bit floating point A.L.U. which perform arithmetic operation which include addition, subtraction, multiplication, division operation and design of universal logic gate with high accuracy, high speed ,less delay and less area.

6. OBJECTIVE

Designing of 32 bit floating point A.L.U. which perform arithmetic operation which include addition

,subtraction, multiplication , division operation and design of universal logic gate with high accuracy, high speed ,less delay and less area.

7. PROPOSED METHODOLOGY

1) Designing of addition/subtraction module.
2) Designing of multiplication module.
3) Designing of Division module.
4) Designing of universal gate module.
5) To study the concept of pipelining, Parallel processing which is used to execute multiple instructions simultaneously
6) Comparison and study of the results

8. PROBABLE OUTCOME

Proposed work will result 32 bit floating point A.L.U. with universal logic gate, which perform addition, subtraction, multiplication, division and designing of universal logic gate. This will meet the following specifications:

- Reduce Area
- Less delay

9. AVAILABLE TOOLS

1) Xilinx

10. CONCLUSION

In this way I will design the 32 bit floating point A.L.U. with universal logic gate, with reduce area, less complexity, and less delay. Because of that capability of A.L.U. increases.

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