"DESIGN OF 4 -BIT ARITHMETIC AND LOGIC UNIT USING GATE DIFFUSION INVERTER TECHNIQUES FOR MINIMUM POWER CONSUMPTION IN DIGITAL SYSTEM"

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ABSTRACT: *Now days in digital circuit design low power and small area are main issues of concern for VLSI designers. GDI Gate diffusion inverter technique of low power digital combinational design. This technique as compare to other currently used logic design styles, allows less power consumption and reduced propagation delay for low-power design of combinatorial digital circuits with minimum number of transistors. But this basic Gate Diffusion Inverter logic style suffers from some practical limitations like swing degradation, fabrication complexity in standard CMOS process and bulk connections. These limitations can be overcome by modified GDI and Full swing GDI techniques. In this Paper presents to design of 4 -bit Arithmetic and Logic Unit by taking the advantage of concept called Gate Diffusion Inverter Technique (GDI). Arithmetic and Logic Unit is the important block to design the embedded and microprocessors. The Arithmetic Unit will do the arithmetic operations, as ADDITION and SUBSTRACTION. The Logic unit will do the logic operations, as AND, OR, XOR and XNOR by using the concept GDI technique.*

Keywords: basic Gate Diffusion Inverter, VLSI, power consumption, propagation delay

1. INTRODUCTION

With improvement in technology and increasing demand of battery operated mobile platforms like laptop, palmtop computers, cellular phones, wireless modems and portable multimedia applications etc has directed the VLSI designers to be more power aware.. The designer's main purpose in the field of digital circuit design is minimization of power consumption. These advancements are responsible for special design techniques for digital circuits distant from conventional CMOS design style. A large part of research has been performed to expand and advance conventional Complementary Metal Oxide Semiconductor (CMOS) techniques for the fabrication of ULTRA low power integrated circuits (ICs). The purpose of this study is to expand a faster, lower power, and reduced area substitute to standard CMOS logic circuits.

In this Paper presents to design of 4 -bit Arithmetic and Logic Unit by taking the advantage of concept called Gate Diffusion Inverter Technique (GDI). Arithmetic and Logic Unit is the important block to design the embedded and microprocessors. The Arithmetic Unit will do the arithmetic operations, as ADDITION and SUBSTRACTION. The Logic unit will do the logic operations, as AND, OR, XOR and XNOR by using the concept GDI technique.

2. RELATED WORK

Meenu Pareek et. al.[1] design an emerging logic style of circuit using the gate diffusion input (GDI) technique. This technique is adopted to design a 32-bit ETA. The proposed design reduces area in terms of area the transistor count to a great extent as well as improves the delay and power performance. Simulation results have shown that proposed design achieves 38% improvement in the Power-Delay-Product when compared to the existing design.

Mrs. Sujatha Hiremath et. al. [2] presents a full adder circuit based on multiplexers, which are implemented using different techniques such as pass transistor, transmission gate and Gate Diffusion Input (GDI). The adder circuits implemented, simulated and comparison results are presented. Cadence tool set using 180 nm technology is used to obtain the results.

B.N. Manjunatha Reddy et. al. [3] presents the GDI technique is used for low-power design of 8-bit multiplier. Reduction in power and area can be achieved using Booth encoding and Wallace tree technique since they generate partial products efficiently and are most suited for multiplication of signed numbers. Multiplier designed in GDI logic requires lesser number of devices as compared to CMOS logic [3]. Hence, GDI multiplier substantially dissipates lesser power as compared to CMOS design.

Arkadiy Morgenshtein et. al. [4] proposed a CMOS compatible Gate Diffusion Input (GDI) design technique. The GDI method enables the implementation of a wide range of complex logic functions using only two transistors. This method is suitable for the design of low-power logic gates, with a much smaller area than Static CMOS and existing PTL techniques. As opposite to our originally proposed GDI logic, the modified GDI logic is fully compatible for implementation in a standard CMOS process. Simulations of basic GDI gates under process and temperature corners in 40 nm CMOS process are shown and compared to similar CMOS gates. They show that while having the same delay, GDI gates achieve leakage and active power reduction of up to 70% and 50%, respectively.

Arkadiy Morgenshtein et. al. [5] analyzes the GDI technique by implementation of logic gates and comparing their properties with their analogues in CMOS and PTL. A variety of logic gates have been implemented in 0.35pm technology and results of the comparison are presented. In order to prove the practical applicability of GDI and display its properties, the prototype test chip of 8-bit CLA Adder has been fabricated in 1.6pm technology, based on GDI and CMOS cell libraries.

3. PROBLEM STATMENT

As the speed of the ALU is the main matter of concern while designing the new and faster processing system or microprocessor. Improved ALU should be faster which in turn to improve the response time of the system. If the speed of ALU increasing the speed of processor will automatically increases. Also the area of the circuit will also reduce as the transistor count in circuit reduces.

4. SYSTEM OBJECTIVE

This project is to design 4-bit Arithmetic Logic Unit (ALU) with mix design technique. With improved Delay in the circuit and possibly reduce the power consumption in circuit. For 4bit ALU operation CMOS technique required – 592 Transistor So to reduce the area in mix technique less number of transistors will needed than CMOS.

Having specifications

• 0.18µm Technology

• Supply Voltage 1.8V

• By Tanner 15.0 EDA Tool

5. SYSTEM DESIGN

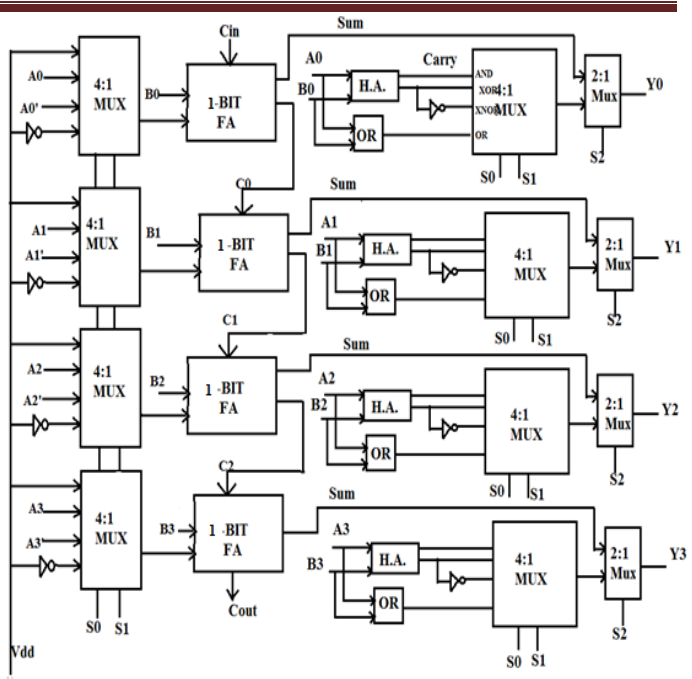

Figure 1: Proposed Architecture of ALU

6. EXPERIMENTAL RESULTS

6.1 HALF ADDER

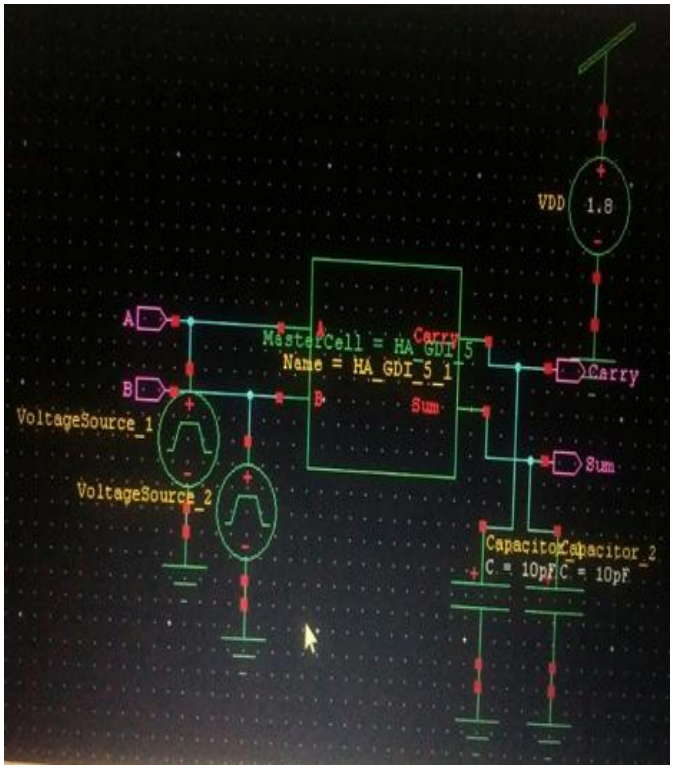

Figure 2: Design Half Adder

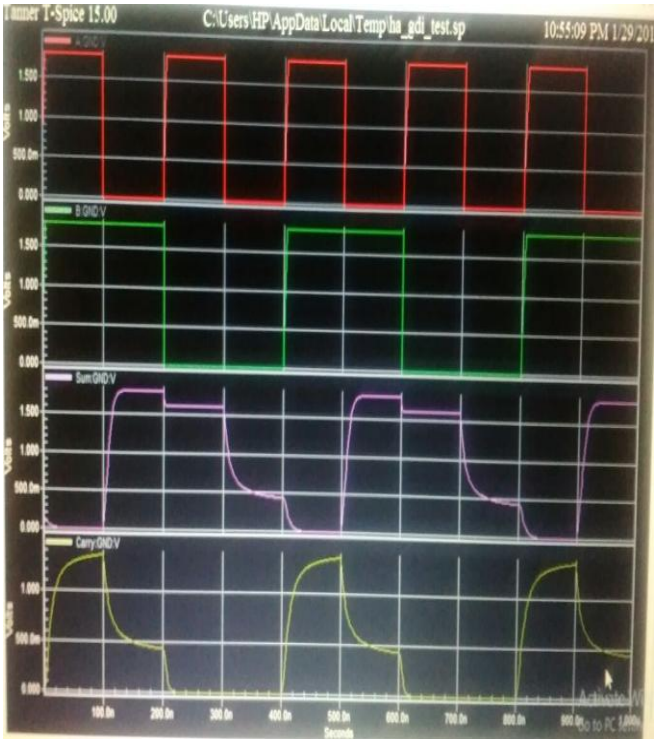

Figure 3: Output waveform of Half Adder

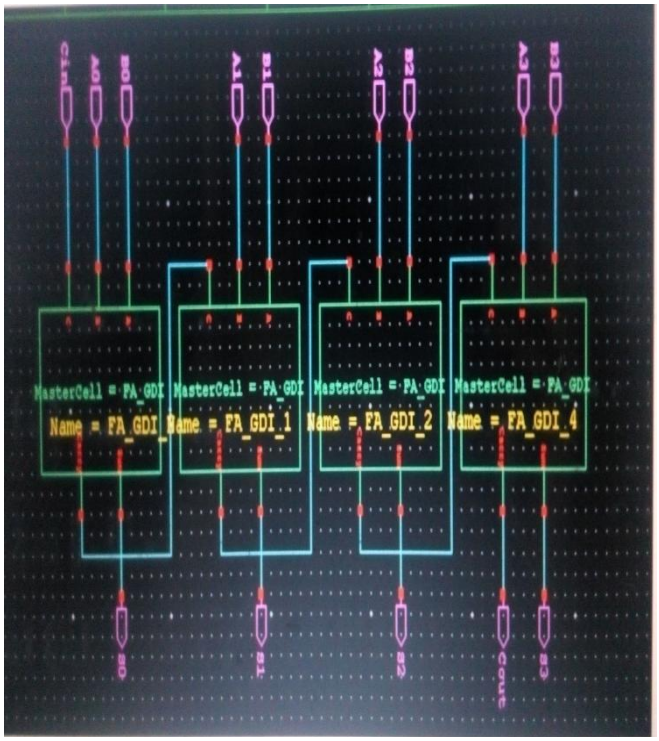

Figure 5: Block diagram of Full Adder

6.2 FULL ADDER

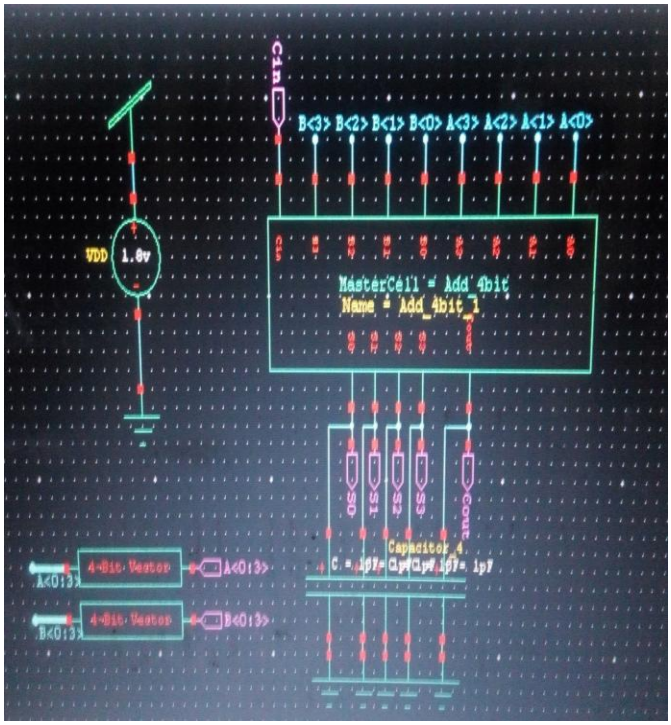

Figure 4: Design of 4 bit Full Adder

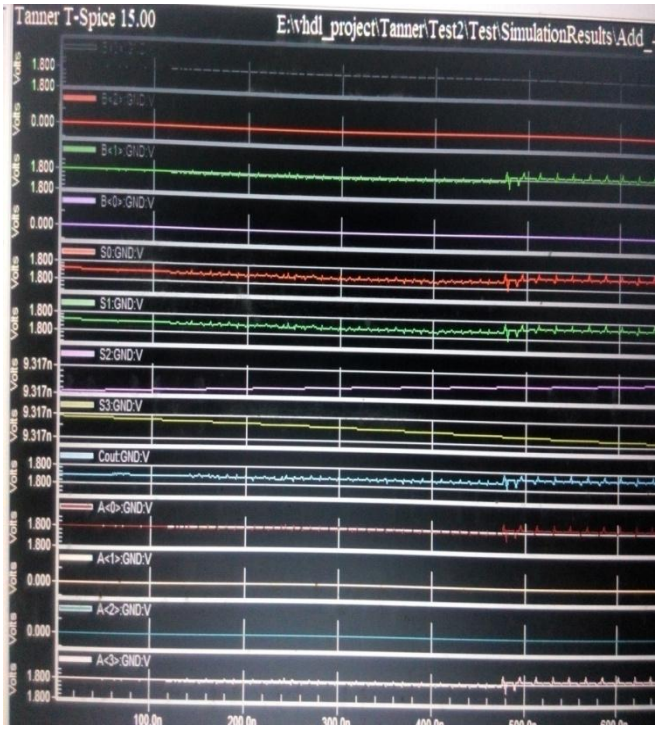

Figure 6: Output wave of 4-bit Full Adder

6.3 4: 1 MUX

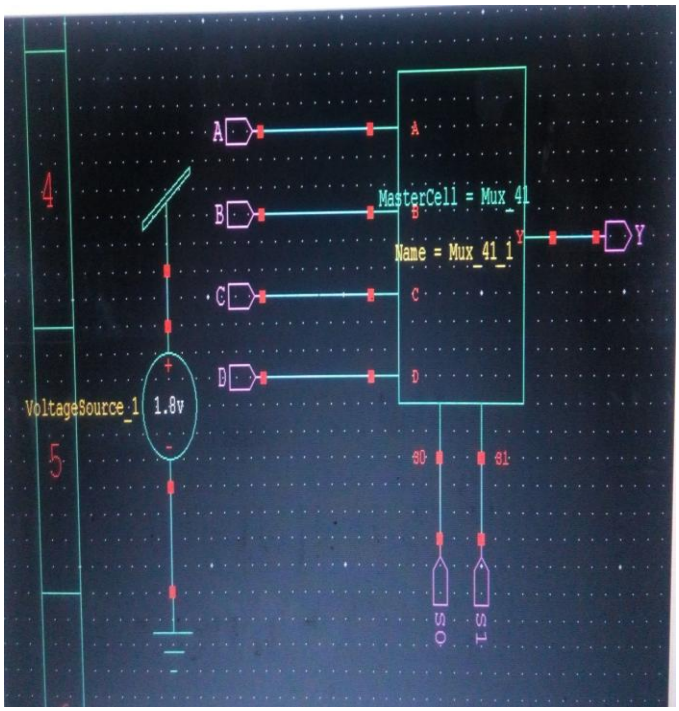

Figure 7: Design 4:1 MUX

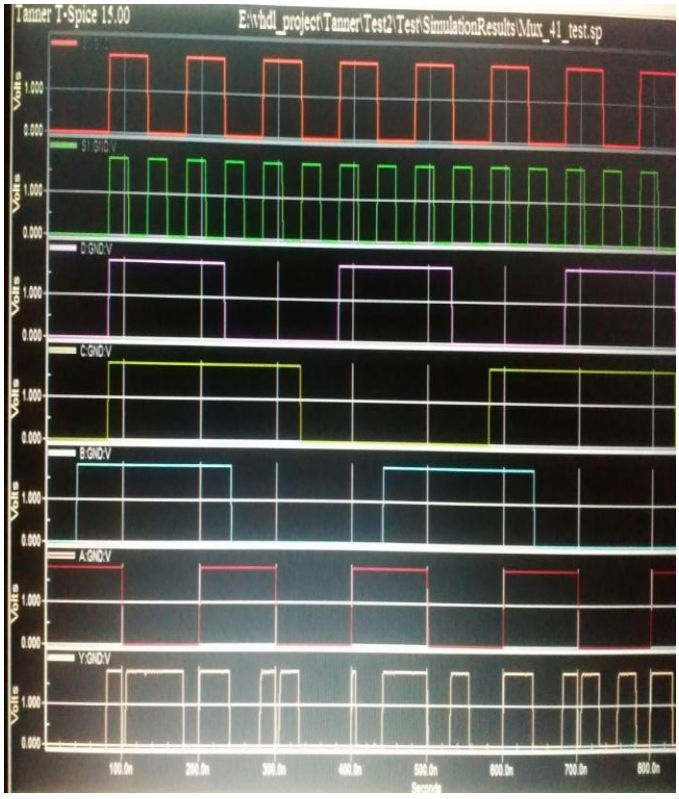

Figure 8: Output waveform of 4:1 MUX

6.4 ALU

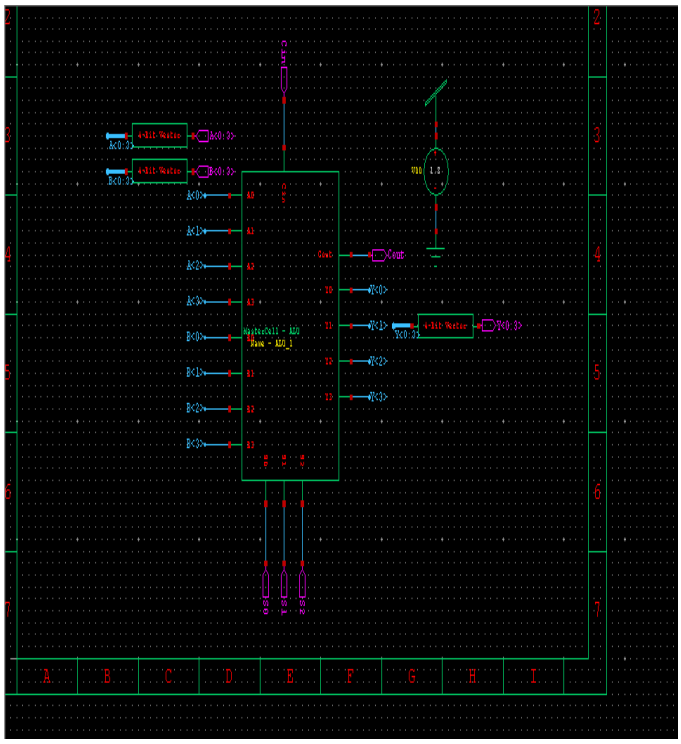

Figure 9: Design 4 bit ALU

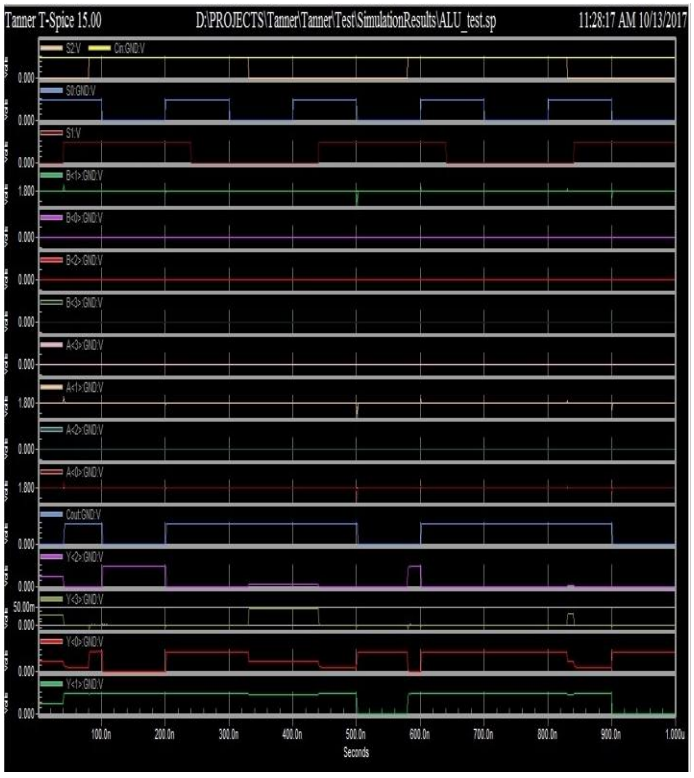

Figure 10: Output waveform of ALU

7. COMPARATIVE ANALYSIS

Sr. No.	Design	No. of Transistor	Power (uW)
1	ALU with CMOS GATE	592	4204.5
2	ALU with Transmission Gate & 10 Transistor Full adder	416	1197.5
3	Proposed ALU with GDI	232	1030.5

Table 1: Comparative Study of the Performance Parameters of 4-Bit ALU

8. CONCLUSION

• The project primarily is focused on the design of optimized delay and high performance 4-Bit ALU. Gate Diffusion Inverter logic style used in this work provides us low power design as compared to CMOS logic styles. It also presents an area efficient approach to low power, as GDI requires less number of transistors as compared to CMOS and TG.
• 4-Bit, ALU is designed using GDI, TG logic styles in which the Full adder is designed by GDI technology and multiplexers are made by TG in TANNER 15.0 EDA Tool SPICE using 180 nm Technology with 1.8 volts as supply voltage.
• It has been observed that TG is most effective in terms of transistor count as it requires less no of transistors, delay and least power consumption in GDI.
• The advantage of GDI technique is two transistor implementation for logic function. Switching activity of TG is too much lower than CMOS hence the delay also optimized so the speed of execution will be more for the system. This together with positive measurement and simulation results, provide evidence that the GDI and TG design might enrich the toolbox of VLSI designers.

9. REFERENCES

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